

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 33

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte SHIGEKI TOMISHIMA

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Appeal No. 1997-1695  
Application 08/496,121

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HEARD: April 20, 2000

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Before RUGGIERO, LALL and BARRETT, Administrative Patent Judges.

RUGGIERO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 23 and 25 through 31. Claim 24 was canceled earlier in the prosecution. An amendment after final rejection filed May 24, 1996 which amended claims 7, 9, 10, 17 through 20, 28, and 30 and canceled claims 11, 14, and 23 was entered by the Examiner. A further amendment after final

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rejection filed

December 19, 1996 which amended claim 10 was also entered by the Examiner. In the final rejection dated March 7, 1996, the Examiner indicted the allowability of claims 7, 9, 17, 18, and 28 through 31 subject to the overcoming of a 35 U.S.C. § 112, second paragraph, rejection. As a result of the amendments after final, the Examiner withdrew the 35 U.S.C. § 112, second paragraph, rejection and, accordingly, the rejection of claims 1 through 6, 8, 10, 12, 13, 15, 16, 19 through 22, and 25 through 27 is before us on appeal.

The claimed invention relates to a boosted potential generating circuit in which a P-channel MOS drive transistor is provided between a first node and a boosted potential node. More particularly, Appellant indicates at pages 14 through 16 of the specification that potential generating circuits provide first and second signals having a precharge potential level and a potential level higher than the precharge potential. These signal are applied to first and second nodes with the applied signals being opposite in phase.

Claim 1 is illustrative of the invention and reads as follows:

1. A boosted potential generating circuit comprising:

a P-channel MOS transistor connected between a first node and a boosted potential node for outputting a boosted potential, said P-channel MOS transistor having a gate electrode connected to a second node;

first potential means for supplying a first signal having a first level of a positive precharge potential and a second level of a potential higher than the precharge potential to said first node; and

second potential means for supplying a second signal having a phase opposite to said first signal supplied by said first potential means and having a third level of the positive precharge potential and a fourth level of a potential higher than the precharge potential to said second node.

The Examiner's Answer cites the following prior art references:<sup>1</sup>

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<sup>1</sup> The Examiner explicitly relies only on Ichimura as the basis for the prior art rejections. The Yilmaz, Truong, and Koford references are cited as

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Ichimura	5,140,182	Aug. 18, 1992
Yilmaz et al. (Yilmaz)	5,426,328	Jun. 20, 1995
		(Filed Apr. 11, 1994)
Truong et al. (Truong)	5,444,405	Aug. 22, 1995
		(Filed Jun. 08, 1994)
Koford et al. (Koford)	5,557,533	Sep. 17, 1996
		(Filed Apr. 19, 1994)

Claims 1 and 10 stand finally rejected under 35 U.S.C.  
§ 102(b) as being anticipated by Ichimura. Claims 4, 5, 13,  
21,  
and 22 stand finally rejected under 35 U.S.C. § 103 as being

unpatentable over Ichimura. In a new ground of rejection in  
the Answer, the Examiner also rejected claims 2, 3, 6, 8, 12,  
15, 16, 19, 20, and 25 through 27 under 35 U.S.C. § 103 as  
being unpatentable over Ichimura.

Rather than reiterate the arguments of Appellant and the  
Examiner, reference is made to the Briefs<sup>2</sup> and Answers for the

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"... evidence to support a position." (Answer, page 3).

<sup>2</sup> The Appeal Brief was filed August 16, 1996. In response to the  
Examiner's Answer dated October 22, 1996, a Reply Brief was filed December 19,  
1996. Supplemental Examiner's Answers were submitted by the Examiner on March

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respective details.

#### OPINION

We have carefully considered the subject matter on appeal, the rejections advanced by the Examiner and the evidence of anticipation and obviousness relied upon by the Examiner as support for the rejections. We have, likewise, reviewed and taken into consideration, in reaching our decision, Appellant's arguments set forth in the Briefs along with the Examiner's rationale in support of the rejections and arguments in rebuttal set forth in the Examiner's Answers.

It is our view, after consideration of the record before us, that Ichimura does not fully meet the invention as set forth in claims 1 and 10. We are also of the view that the evidence relied upon and the level of skill in the particular art would not have suggested to one of ordinary skill in the art the obviousness of the invention as recited in claims 2 through 6, 8, 12, 13, 15, 16, 19 through 22, and 25 through 27.

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7, 1997 and July 31, 1997 which indicated entry of the Reply Brief.

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Accordingly, we reverse.

We consider first the rejection of claims 1 and 10 under 35 U.S.C. § 102(b) as being anticipated by Ichimura. Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied Digital Data Systems, Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.); cert. dismissed, 468 U.S. 1228 (1984); W.L. Gore and Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

With respect to independent claim 1, the Examiner attempts to read the claimed limitations on the booster circuit illustrated in Figure 1 of Ichimura. In the Examiner's view (Answer, page 4), the transistor QB on the far right of Ichimura's Figure 1 corresponds to the claimed PMOS drive transistor and the unillustrated potential means which supply the

NC and ND clock signals correspond to the claimed first and second potential means. The Examiner also makes note of the fact that, although Ichimura's transistor QB is illustrated and described as an N-channel transistor, Ichimura expressly provides (column 10, lines 1-6) for replacing the N-channel transistors with P-channel transistors.

In response, Appellant's arguments center on two alleged primary differences between Ichimura's disclosed booster circuit and the claimed invention. Initially, Appellant contends (Brief, page 10) that Ichimura's express disclosure of the drive transistor QB in Figure 1 is of an N-channel type, not a P-channel type as claimed. We do not find such contention to be well founded. In our view, to accept Appellant's argument, one would have to ignore the clear, unambiguous disclosure at column 10, lines 1-4 of Ichimura which states:

... although N channel MOS transistors  
or the like are used for each element in  
the above embodiments, P channel MOS  
transistors, bipolar transistors, diodes  
or the like also may be appropriately used.

Appellant's second major point of argument asserts a lack of disclosure in Ichimura of the claimed requirement that the

signals applied to the input and gate electrodes of Ichimura's

drive transistor QB be opposite in phase. Although we found Appellant's argument concerning Ichimura's lack of disclosure of a PMOS drive transistor to be without merit, we reach the opposite conclusion regarding the opposite phase drive transistor input signals. After careful consideration of the Ichimura reference in light of the arguments of record, we are in agreement with Appellant's stated position in the Briefs. As discussed supra, the Examiner has identified the signals identified as waveforms NC and ND (Ichimura, Figures 1 and 2) as corresponding to the first and second signals produced by the claimed first and second potential means. It is apparent to us, however, from the illustration in Figure 2 and the accompanying description at columns 7 and 8 of Ichimura that the signals NC and ND are not opposite in phase as claimed.

We note that the Examiner, in responding to this last argument of Appellant and reiterating that Ichimura expressly provides for substituting P-channel transistors for N-channel transistors, asserts (Answer, page 9) the following:

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... since it would have been clearly understood by one skilled in the art (i.e., inherent) that the change in conductivity type would correspondingly require a change in the phase between signals NC and ND, it is seen that Ichimura anticipates the claimed invention.

The record in this case, however, is totally devoid of any support for such a position. We are not inclined to dispense with proof by evidence when the proposition at issue is not supported by a teaching in a prior art reference, common knowledge or capable of unquestionable demonstration. Our reviewing court requires this evidence in order to establish a prima facie case. In re Knapp-Monarch Co., 296 F.2d 230, 232, 132 USPQ 6, 8 (CCPA 1961); In re Cofer, 354 F.2d 664, 668, 148 USPQ 268, 271-72 (CCPA 1966). In our view, while it is generally true that N-channel transistors turn on when the gate voltage is higher than the source voltage, and vice-versa for P-channel transistors, this does not lead to the conclusion that the signals applied to the transistor input and gate electrodes must necessarily be opposite in phase. As discussed supra, the clock signals NC and ND, which are

applied to opposite sides of transistor QB in Ichimura are clearly shown not to be opposite in phase. In our view, the Examiner has provided no persuasive evidence to indicate that an opposite phase relationship of these input signals would necessarily be established if a P-channel, rather than an N-channel, transistor was utilized as the drive transistor in Ichimura's booster circuit.

In view of the above discussion, since all of the claimed limitations are not disclosed by Ichimura, we do not sustain the Examiner's 35 U.S.C. § 102(b) rejection of claims 1 and 10.

Turning to a consideration of the obviousness rejection of claims 2 through 6, 8, 12, 13, 15, 16, 19 through 22, and 25 through 27 based on Ichimura, we do not sustain this rejection as well. With respect to independent claims 12 and 20, the Examiner reiterates his position discussed previously with regard to the 35 U.S.C. § 102(b) rejection of independent claim 10. In addition, the Examiner asserts the obviousness to the skilled artisan of utilizing buffers to generate system clock signals as recited in claim 12 as well as the use of series connected inverters as buffer circuitry as recited in

claim 20. We note, however, that each of independent claims 12 and 20 include the requirement that the applied signals to the drive transistor be opposite in phase, a feature which we found lacking in Ichimura as discussed supra. Accordingly, because the Examiner has not established a prima facie case of obviousness since all of the limitations of the claims are not taught or suggested by the prior art, the 35 U.S.C. § 103 rejection of independent claims 12 and 20 as well as dependent claims 2 through 6, 8, 14 through 16, 19, 21, 22, and 25 through 27 is not sustained.

Finally, we have reviewed the Truong, Yilmaz, and Koford references cited in the Answer as evidentiary support for the Examiner's assertion of the well known aspects of buffer generated clock signals (Truong) and single chip architecture (Yilmaz and Koford). We find no disclosure in any of the references which would overcome the innate deficiencies of Ichimura in disclosing the application of input signals to a drive transistor which are opposite in phase.

In summary, we have not sustained either of the Examiner's rejections of the claims on appeal. Accordingly,

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the Examiner's decision to reject claims 1 through 6, 8, 10,  
12, 13, 15, 16, 19 through 22, and 25 through 27 is reversed.

REVERSED

LEE E. BARRETT	)	
Administrative Patent Judge	)	
	)	
	)	
	)	BOARD OF PATENT
JOSEPH F. RUGGIERO	)	APPEALS AND
Administrative Patent Judge	)	INTERFERENCES
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	)	
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PARSHOTAM S. LALL	)	
Administrative Patent Judge	)	

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